Q.P. Code: 18EC0431 **R18**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech IV Year I Semester Regular Examinations February-2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

PART-A

(Answer all the Questions **5 x 2 = 10** Marks)

1	a	Define Threshold Voltage of the MOS transistor	L1	2M
	b	Illustrate nMOS transistor in λ-based design rule.	L2	2M
	c	Briefly describe Switch logic	L1	2M
	d	What are the high-density memory elements? Explain in brief.	L2	2M
	e	What is the need of Testing?	L1	2M

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	Illustrate about basic MOS transistors	L2	4M
	b	Show the circuit diagram of a simple BiCMOS inverter and explain its operation.	L1	6M

OR

3		Illustrate the steps involved in nMOS fabrication process with neat sketches.	L2	10M

UNIT-II

4	a	Explain the steps involved in VLSI Design flow.	L2	5M
	b	Construct the stick diagram of a 2-input CMOS NAND gate.	L3	5M

OR

5	a	Construct stick diagram for $Y = \overline{(AB + CD)}$ in NMOS design style.	L3	5M
	b	Construct the layout diagram for 2-input CMOS NOR gate.	L3	5M

UNIT-III

6	a	Sketch 2 x 1 mux using transmission gates.	L3	5M
	b	What is pseudo NMOS logic? Explain with an example	L1	5M

OR

7		Explain the following terms (i) Floor planning (ii) Placement (iii) Routing	L2	10M

UNIT-IV

8		Construct and explain the ripple counter with neat sketches.	L1	10M

OR

9		Explain in detail about 6-transistor Static memory cell.	L2	10M

UNIT-V

10	a	Give a logic circuit example in which stuck-at-1 fault and stuck-at-0 fault are indistinguishable.	L2	5M
	b	What is FPGA? Draw and explain basic structure of FPGA.	L1	5M

OR

11	a	Discuss about the Fault coverage and how to find it.	L1	5M
	b	Explain Chip Level Test techniques and its methodology.	L2	5M

END